Exhibit 2: Correspondence between Claims of Bailey and Proposed Counts

I. Claims 1-17 of Bailey correspond to Proposed Count 1

Applicant respectfully submits that claims 1-17 of Bailey correspond to proposed count 1 as discussed below:

Claim 1	Correspondence to Count 1 and Remarks
A microprocessor comprising:	corresponds to "A microprocessor comprising:"
a CPU core capable of executing a predetermined instruction set;	corresponds to "a processor unit;"
a clock generator and distribution unit coupled to said CPU core, wherein said clock generator and distribution unit is configured to provide a CPU clock signal to said CPU core, and wherein a frequency of said CPU clock signal is dependent upon a frequency of a timing signal; and	corresponds to "a clock circuit providing a clock signal to the processor unit, the clock signal having an associated frequency;"
a clock control circuit coupled to said clock generator and distribution unit, wherein said clock control circuit includes:	corresponds to the "means for varying the associated frequency of the clock signal in response to at least one of the first and second signals"
a frequency control circuit configured to selectively vary a frequency of said timing signal depending upon a control signal;	
a thermal sensor capable of providing a temperature signal indicative of a temperature associated with said microprocessor;	corresponds to "a thermal sensor generating a temperature signal corresponding to a temperature of the microprocessor;"
a primary temperature indicator unit coupled to said thermal sensor, wherein said primary temperature indicator unit is capable of asserting a primary indicator signal if said temperature signal exceeds a first predetermined threshold level;	corresponds to the "logic circuitry coupled to the thermal sensor, the logic circuitry generating a first signal if the temperature signal exceeds a first threshold level and a second signal if the temperature signal exceeds a second threshold level"
an auxiliary temperature indicator unit coupled to said thermal sensor and capable of asserting an auxiliary indicator signal if said temperature signal exceeds a second predetermined threshold level; and	

Claim 1 continued on next page

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Claim 1 (continued)	Correspondence to Count 1 and Remarks
a clock management unit coupled to receive said primary indicator signal and said auxiliary indicator signal, and coupled to said frequency control circuit, wherein said clock management unit is configured to vary said control signal to thereby cause a change in the frequency of said timing signal in response to assertions of said primary indicator signal and said auxiliary indicator signal.	corresponds to the "means for varying the associated frequency of the clock signal in response to at least one of the first and second signals"

Claim 2	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 1 wherein said primary temperature indicator unit is associated with a hysteresis characteristic whereby, upon assertion of said primary indicator signal, said primary indicator signal remains asserted until said temperature signal has dropped below a first predetermined hysteresis point associated with said primary temperature indicator unit.	One definition of "hysteresis" is "The tendency of a system, a device, or a circuit to behave differently depending on the direction of change of an input parameter. *A household thermostat demonstrates hysteresis: When the temperature is decreasing, the thermostat might turn on at 68 degrees, but when the temperature is warming, it might turn off at 72 degrees, Without hysteresis, the thermostat might turn off and on at the same temperature and would therefore oscillate rapidly." (emphasis added)*(*see, e.g.*, "hysteresis" excerpt from the MS Press Computer Dictionary, 2d ed. 1994). Applicant respectfully submits that the use of hysteresis in temperature control circuitry is well known in the art. Applicant submits that claim 2 of Bailey is not patentably distinct from claim 1 and thus corresponds to proposed count 1.

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Claim 3	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 2 wherein said auxiliary temperature indicator unit is associated with a hysteresis characteristic whereby, upon assertion of said auxiliary indicator signal, said auxiliary indicator signal remains asserted until said temperature signal has dropped below a second predetermined hysteresis point associated with said auxiliary temperature indicator unit.	As stated above with respect to claim 2, applicant respectfully submits that the use of hysteresis in temperature control circuitry is well known in the art. Therefore claim 3 of Bailey corresponds to and is not patentably distinct from proposed count 1.

Claim 4	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 1 wherein said clock management unit is configured to control said frequency control circuit such that said timing signal is associated with a first predetermined frequency if said primary indicator signal and said auxiliary indicator signal are asserted, and such that said timing signal is associated with a second predetermined frequency if said auxiliary indicator signal is asserted while said primary indicator signal is deasserted, and such that said timing signal is associated with a third predetermined frequency if said auxiliary indicator signal is deasserted, wherein said first predetermined frequency is lower than said second predetermined frequency, and wherein said second predetermined frequency is lower than said third predetermined frequency.	Applicant submits that a circuitry that varies the clock frequency in response to various combinations of the primary and auxiliary signals is not patentably distinct from "means for varying the associated frequency of the clock signal in response to at least one of the first and second threshold signals" of count 1. Applicant thus submits that claim 4 corresponds to and is not patentably distinct from proposed count 1.

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Claim 5	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 1 wherein said frequency control circuit includes a phase locked loop circuit coupled to said clock management unit.	Applicant submits that the use of phase locked loop circuits for generating and controlling clock signal frequencies is well known in the art. (see, e.g., Horowitz, et al., "Phase-Locked Loops", The Art of Electronics, pp. 641-655, 1989 at §§ 9.29, 9.31). Thus claim 5 corresponds to and is not patentably distinct from proposed count 1.

Claim 6	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 5 wherein said phase locked loop circuit generates an output signal which is associated with a predetermined factor of a frequency of an external clock signal provided to said phase locked loop circuit, wherein said timing signal is derived from said output signal.	Applicant submits that the use of phase locked loop circuit for generating and controlling clock signal frequencies is well known in the art. (see, e.g., Horowitz, et al., "Phase-Locked Loops", The Art of Electronics, pp. 641-655, 1989 at §§ 9.29, 9.31). Thus claim 6 corresponds to and is not patentably distinct from proposed count 1.

Claim 7	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 6 further comprising a divider circuit for receiving said output signal of said phase locked loop circuit and for deriving said timing signal.	Applicant submits that the use of phase locked loop circuits for generating and controlling clock signal frequencies is well known in the art. (see, e.g., Horowitz, et al., "Phase-Locked Loops", The Art of Electronics, pp. 641-655, 1989 at §§ 9.29, 9.31). Applicant further submits that the use of frequency dividers to generate a clock signal from a higher frequency signal is well known in the art. (see, e.g., Horowitz, et al., "Divide by more", The Art of Electronics, pp. 511-513, 1989.) Applicant thus respectfully submits that claim 7 corresponds to and is not patentably distinct from proposed count 1.

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Claim 8	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 1 further comprising a programmable registers unit coupled to said primary temperature indicator unit and to said auxiliary temperature indicator unit, wherein said programmable registers unit is capable of storing said first and second predetermined threshold levels.	Applicant respectfully submits that the use of a register to store values in a microprocessor is well known in the art. Proposed count 1 includes the language: "logic circuitry coupled to the thermal sensor, the logic circuitry generating a first signal if the temperature signal exceeds a first threshold level and a second signal if the temperature signal exceeds a second threshold level" Applicant submits that storing the threshold levels in a register does not render claim 8 patentably distinct from proposed count 1.

Claim 9	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 8 further comprising a bus coupled to said CPU core and to said programmable registers unit wherein said programmable registers unit may be written via said bus.	Applicant respectfully submits that the use of a bus to couple a processor unit to a register in a microprocessor is well known in the art. Applicant thus submits that writing the threshold levels in a register via a bus does not render claim 9 patentably distinct from proposed count 1.

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Claims of Bailey and Proposed Counts

Claim 10	Correspondence to Count 1 and Remarks
The microprocessor as recited in claim 1 wherein said temperature signal provided from said thermal sensor is indicative of a temperature of a semiconductor die on which said microprocessor is fabricated.	Applicant submits that proposed count 1 includes the language "a thermal sensor generating a temperature signal corresponding to a temperature of the microprocessor" Applicant submits that the temperature of the semiconductor die is a temperature of the microprocessor contemplated by the applicant (see pg. 23, lines 18-26). Thus applicant submits that claim 10 of Bailey is not patentably distinct from proposed count 1.

Claim 11	Correspondence to Count 1 and Remarks
11. A clock control circuit for providing a timing signal that controls an internal clock frequency of a microprocessor, said clock control circuit comprising:	corresponds to "A microprocessor comprising:"
a frequency control circuit configured to selectively vary a frequency of said timing signal depending upon a control signal;	corresponds to the "means for varying the associated frequency of the clock signal"
a thermal sensor capable of providing a temperature signal indicative of a temperature associated with the said microprocessor;	corresponds to "a thermal sensor generating a temperature signal corresponding to a temperature of the microprocessor"
a primary temperature indicator unit coupled to said thermal sensor, wherein said primary temperature indicator unit is capable of asserting a primary indicator signal if said temperature signal exceeds a first predetermined threshold level;	corresponds to "logic circuitry coupled to the thermal sensor, the logic circuitry generating a first signal if the temperature signal exceeds a first threshold level and a second signal if the temperature signal exceeds a second threshold level"
an auxiliary temperature indicator unit coupled to said thermal sensor and capable of asserting an auxiliary indicator signal if said temperature signal exceeds a second predetermined threshold level; and	

Claim 11 continued on next page

Exhibit 2: Correspondence between
Claims of Bailey and Proposed Counts

Claim 11 (continued)	Correspondence to Count 1 and Remarks
a clock management unit coupled to receive said primary indicator signal and said auxiliary indicator signal, and coupled to said frequency control circuit, wherein said clock management unit is configured to vary said control signal to thereby cause a change in the frequency of said timing signal in response to assertions of said primary indicator signal and said auxiliary indicator signal.	corresponds to the "means for varying the associated frequency of the clock signal in response to at least one of the first and second signals"

Claim 12	Correspondence to Count 1 and Remarks
The clock control circuit as recited in claim 11 wherein said primary temperature indicator unit is associated with a hysteresis characteristic whereby, upon assertion of said primary indicator signal, said primary indicator signal remains asserted until said temperature signal has dropped below a first predetermined hysteresis point associated with said primary temperature indicator unit.	As stated above with respect to claim 2, applicant submits that the use of hysteresis in temperature control circuitry is well known in the art. (*see, e.g.*, "hysteresis" excerpt from the MS Press Computer Dictionary, 2d ed. 1994). Applicant respectfully submits that claim 12 corresponds to and is not patentably distinct from proposed count 1.

Claim 13	Correspondence to Count 1 and Remarks
The clock control circuit as recited in claim 12 wherein said auxiliary temperature indicator unit is associated with a hysteresis characteristic whereby, upon assertion of said auxiliary indicator signal, said auxiliary indicator signal remains asserted until said temperature signal has dropped below a second predetermined hysteresis point associated with said auxiliary temperature indicator unit.	As stated above with respect to claim 2, applicant submits that the use of hysteresis in temperature control circuitry is well known in the art. (*see, e.g.*, "hysteresis" excerpt from the MS Press Computer Dictionary, 2d ed. 1994). Applicant respectfully submits that claim 13 corresponds to and is not patentably distinct from proposed count 1.

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Claim 14	Correspondence to Count 1 and Remarks
The clock control circuit as recited in claim 11 wherein said clock management unit is configured to control said frequency control circuit such that said timing signal is associated with a first predetermined frequency if said primary indicator signal and said auxiliary indicator signal are asserted, and such that said timing signal is associated with a second predetermined frequency if said auxiliary indicator signal is asserted while said primary indicator signal is deasserted, and such that said timing signal is associated with a third predetermined frequency if said auxiliary indicator signal is deasserted, wherein said first predetermined frequency is lower than said second predetermined frequency, and wherein said second predetermined frequency is lower than said third predetermined frequency.	Applicant submits that circuitry to select specific frequencies of the clock signal in response the status of the two (primary and auxiliary) signals is not patentably distinct from "means for varying the associated frequency of the clock signal in response to at least one of the first and second signals" of proposed count 1. Thus claim 14 corresponds to and is not patentably distinct from proposed count 1.

Claim 15	Correspondence to Count 1 and Remarks
The clock control circuit as recited in claim 11 wherein said frequency control circuit includes a phase locked loop circuit coupled to said clock management unit.	Applicant submits that the use of a phase locked loop circuit for generating and controlling clock signal frequencies is well known in the art. (see, e.g., Horowitz, et al., "Phase-Locked Loops", The Art of Electronics, pp. 641-655, 1989 at §§ 9.29, 9.31). Thus claim 15 is not patentably distinct from proposed count 1.

Claim 16	Correspondence to Count 1 and Remarks
The clock control circuit as recited in claim 15 wherein said phase locked loop circuit generates an output signal which is associated with a predetermined factor of a frequency of an external clock signal provided to said phase locked loop circuit, wherein said timing signal is derived from said output signal.	Applicant submits that the use of phase locked loop circuit for generating and controlling clock signal frequencies from another clock signal is well known in the art. (see, e.g., Horowitz, et al., "Phase-Locked Loops", The Art of Electronics, pp. 641-655, 1989 at §§ 9.29, 9.31). Thus claim 16 is not patentably distinct from proposed count 1.

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Claim 17	Correspondence to Count 1 and Remarks
The clock control circuit as recited in claim 16 further comprising a divider circuit for receiving said output signal of said phase locked loop circuit and deriving said timing signal.	Applicant submits that the use of a frequency divider to generate a clock signal from a higher frequency signal is well known in the art. (see, e.g., Horowitz, et al., "Divide by more", The Art of Electronics, pp. 511-513, 1989.) Thus claim 17 is not patentably distinct from proposed count 1.

II. Claims 18-20 of Bailey Correspond to Proposed Count 2

Applicant respectfully submits that claims 18-20 of Bailey correspond to proposed count 2 as discussed below.

Claim 18	Correspondence to Count 2 and Remarks
A method for controlling a frequency of an internal clock signal which drives a microprocessor comprising the steps of:	corresponds to "A method of controlling a frequency of a clock signal which drives a microprocessor, comprising the steps of:"
generating a temperature signal indicative of a temperature associated with said microprocessor;	corresponds to "a) generating a temperature signal corresponding to a temperature of the microprocessor;"
comparing said temperature signal with a first predetermined threshold level;	corresponds to "b) generating a first threshold signal if the temperature signal indicates that the microprocessor temperature has exceeded a first threshold temperature;" Applicant submits that Bailey's comparison step is inherent with the "if" test and unnecessarily redundant given that the "if" test appears in the subsequent "asserting" step.
asserting a primary indicator signal if said temperature signal exceeds said first predetermined threshold level;	

Claim 18 continued on next page

Exhibit 2: Correspondence between
Claims of Bailey and Proposed Counts

Claim 18 (continued)	Correspondence to Count 2 and Remarks
comparing said temperature signal with a second predetermined threshold level;	corresponds to "c) generating a second threshold signal if the temperature signal indicates that the microprocessor temperature has exceeded a second threshold temperature." Applicant submits that Bailey's comparison step is inherent with the "if" test and unnecessarily redundant given that the "if" test appears in the subsequent "asserting" step.
asserting an auxiliary indicator signal if said temperature signal exceeds said second predetermined threshold level;	
decreasing a frequency of said internal clock signal if said primary indicator signal is asserted; and	corresponds to "d) varying a frequency of the clock signal in response to at least one of the first and second threshold signals."
increasing said frequency of said internal clock signal if neither said primary indicator signal nor said auxiliary indicator signal are asserted.	

Claim 19	Correspondence to Count 2 and Remarks
The method for controlling a frequency of an internal clock signal as recited in claim 18 comprising the further step of programming said first predetermined threshold level and said second predetermined threshold level within a programmable registers unit.	Applicant submits that the use of registers in a microprocessor to store values is well known in the art. The applicant submits that storing the first and second threshold levels in register(s) is not patentably distinct from proposed count 2.

Claim 20	Correspondence to Count 2 and Remarks
The method for controlling a frequency of an internal clock signal as recited in claim 18 comprising the further step of driving said internal clock signal at an intermediate frequency if said auxiliary indicator signal is asserted and said primary indicator signal is deasserted.	Applicant submits claim 20 is not patentably distinct from "varying a frequency of the clock signal in response to at least one of the first and second threshold signals" as found in proposed count 2.